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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,799	04/02/2004	Robert Warren	STMI08-00007	9934

7590 04/17/2006

Docket Clerk
P.O. Box 802432
Dallas, TX 75380

EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,799	WARREN, ROBERT	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-13 and 15-20* is/are rejected.

7)☒ Claim(s) *3 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2004 and 16 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to Amendments and Remarks filed on 02/16/2006 regarding application 10/816,799 filed on 04/02/2004. Claims 1 – 20 remain pending in the application.

Claim Objections

2. Claims listed below are objected to because of the following informalities:

Claim 8, line 2, change "an unknown state" to —the unknown state—.

Claim 14, line 3, change "the clock cycle" to —a clock cycle—.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 7 – 13 and 15 – 20 are rejected under 35 U.S.C. 102(b) as being unpatentable over U.S. Patent No. 6,353,906 B1 to *Smith et al.*

5. As to Claim 1, *Smith et al.* show and disclose the following subject matter:

- A method of testing and ensuring *proper synchronization* of a signal passing in a circuit, which having a plurality of functional elements (e.g., flip-flops) from one clock domain (clock environment) to another clock domain – [abstract; col. 1, line 5 – 10; Fig. 2];
- Digital simulator – [col. 1, line 7]; Simulation process – [col. 1, line 27 – 28]; Modeling a known asynchronous input signal which violate setup time and hold time requirement of a flip-flop (functional element) to generate a *X transition* (i.e., unknown state) output – [col. 2, line 9 – 24; col. 4, line 43 – col.

5, line 11]; Notice that each of the setup time and hold time is predetermined time after a clocking edge (i.e., timing event) of a clock signal);

- Constructing synchronizers using different number of functional elements (i.e., flip-flops) – [Fig. 2]; Determining which synchronizer, which has non-sufficient number of functional elements (flip-flops), has a synchronization problem for a signal passing from one clock domain to another clock domain – col. 3, line 66 – col. 4, line 42].

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

6. As to Claims 2 and 7, *Smith et al.* show and disclose simulating using clocks signals having different frequencies – [Fig. 3; Fig. 4].

7. As to Claim 8, it is well known in the art that the unknown state propagates through only a part of circuit that following the function element (flip-flop) generating the unknown state.

8. As to Claim 9, reasons are included in **[Response A]** given above. Notice that it is a standard scheme using warnings to identify a function element that is a source of unknown state.

9. As to Claim 10, to simulate various asynchronous conditions, simulating and determining steps should be repeated a plurality of times.

10. As to Claims 11 and 12, reasons are included in **[Response A]** given above. *Smith et al.* show in Fig. 2 and disclose that a combination of flip-flop is a hazard or a synchronizer dependent upon its synchronization capability. A synchronizer should have a sufficient number of flip-flops in order to achieve proper synchronization.

11. As to Claim 13, reasons are included in **[Response A]** given above. Notice that if a first flip-flop is a source generating a unknown state, a second flip-flop should be arranged to avoid the unknown state from propagating.

12. As to Claims 15, 19 and 20, reasons are included in **[Response A]** given above. Notice that functional elements in the circuit are flip-flops, which are represented by logic gates (i.e., in a gate level representation).

13. As to Claims 16 and 17, *Smith et al.* disclose using a simulator (i.e., simulation tool) to simulate a circuit design in HDL description – [col. 1, line 27 – 29].

14. As to Claim 18, reasons are included in **[Response A]** given above.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

16. Claims 4 – 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,353,906 B1 to *Smith et al.* in view of U.S. Patent No. 6,473,439 B1 to *Zerbe et al.*

17. As to Claims 4 – 6, *Smith et al.* teach simulating a synchronization problem existing in a synchronizer design using two clock signals having different frequencies; they do not disclose a simulation using two clock signals having the same frequency and different phases. But *Zerbe et al.* disclose this subject matter – [Fig. 10; abstract; col. 10, line 12 – 35]. It is well known in the art that a synchronization problem also

exists in a synchronizer design for a circuit using two clock signals having different frequencies. Combination of the teachings of *Smith et al.* and *Zerbe et al.*, provides a designer a complete picture and guidelines in design of a synchronizer for a circuit using clock signals having a variety of frequencies and phases.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Zerbe et al.* in order to achieve a complete picture and guidelines for use in design of a synchronizer for a circuit using clock signals having a variety of frequencies and phases.

Notice that different phases include a combination of phase differences between two clock signals of same frequency, as long as phases are not the same.

Allowable Subject Matter

18. Claims 3 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Those claims are allowed is because that the prior art does not teach or fairly suggest the following subject matter:

- A method of testing a circuit under design having a plurality of functional elements and having a plurality of clock environments, at least one signal passing from one clock environment to another clock environment in the circuit, the method comprising a simulation step, wherein the one clock environment and the other clock environment have the same clock frequency and same phase in combination with other limitations recited in **Claim 3;** respectively;
- A method of testing a circuit under design having a plurality of functional elements and having a plurality of clock environments, at least one signal passing from one clock environment to another clock environment in the circuit, the method comprising a step of determining propagation of an unknown state for the remainder of a clock cycle by presence of different values before and after the unknown state presented at an input of a synchronizer in combination with other limitations recited in **Claim 14**.

Response to Amendment and Remarks

19. Applicant's amendments & remarks filed on 02/16/2006 have been reviewed. Since applicant does not response to examiner's concerns recited in the Examiner's Remarks of the Office Action mailed 12/30/2005, responses in the aforementioned Office Action are reversed based on newly found prior art. Detailed responses are given as above.

Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Sun James Lin* whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Jack Chiang* can be reached on (571) 272 - 7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Primary Examiner
Art Unit 2825
April 13, 2006

SUN JAMES LIN
PRIMARY EXAMINER

Docket No.: STMI08-00007
Applicant: Robert Warren.
Serial No.: 10/816,799
Filing Date: April 2. 2004

REPLACEMENT SHEET

Figure 1a

RELATED ART

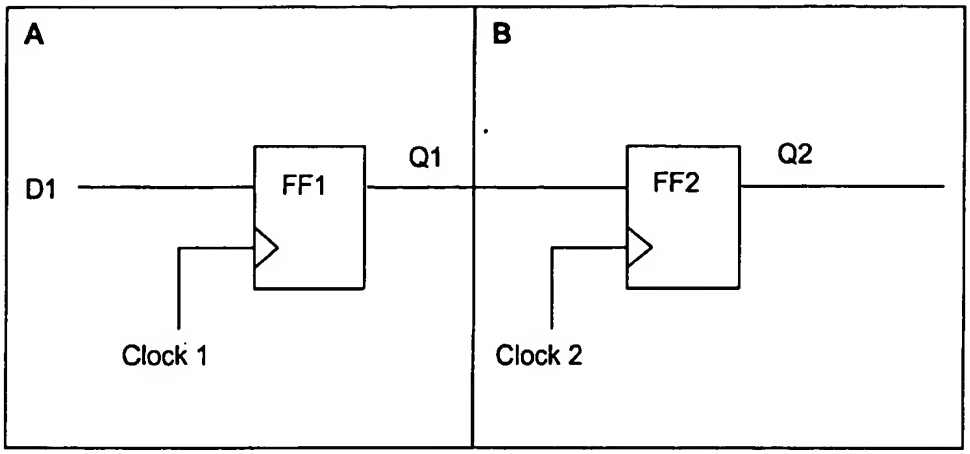
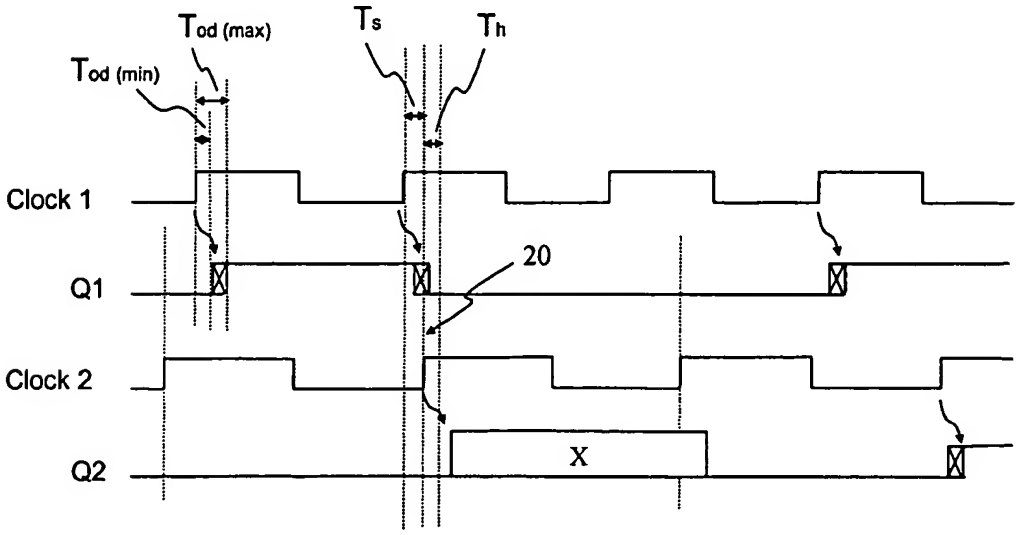


Figure 1b

RELATED ART



Docket No.: STMI08-00007
Applicant: Robert Warren.
Serial No.: 10/816,799
Filing Date: April 2, 2004

REPLACEMENT SHEET

REVIEWED
OK
JRS
2-27-06

Figure 2a

RELATED ART

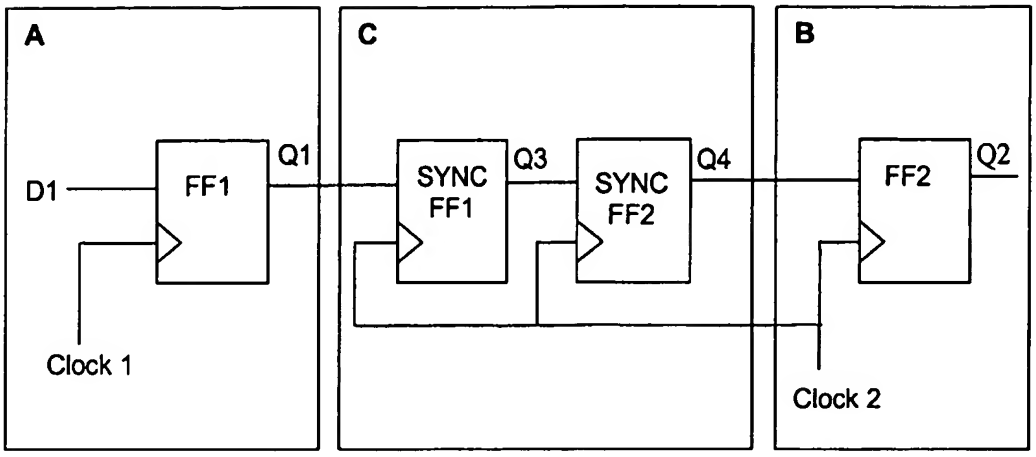


Figure 2b

RELATED ART